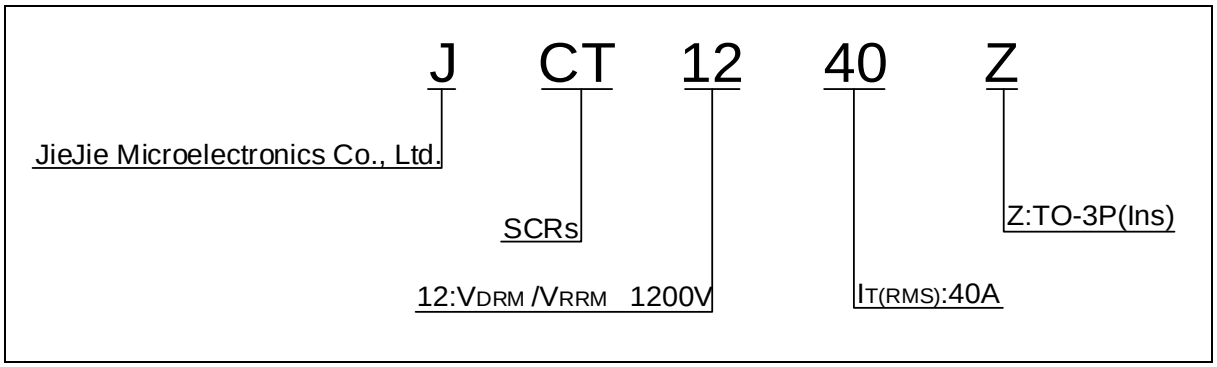
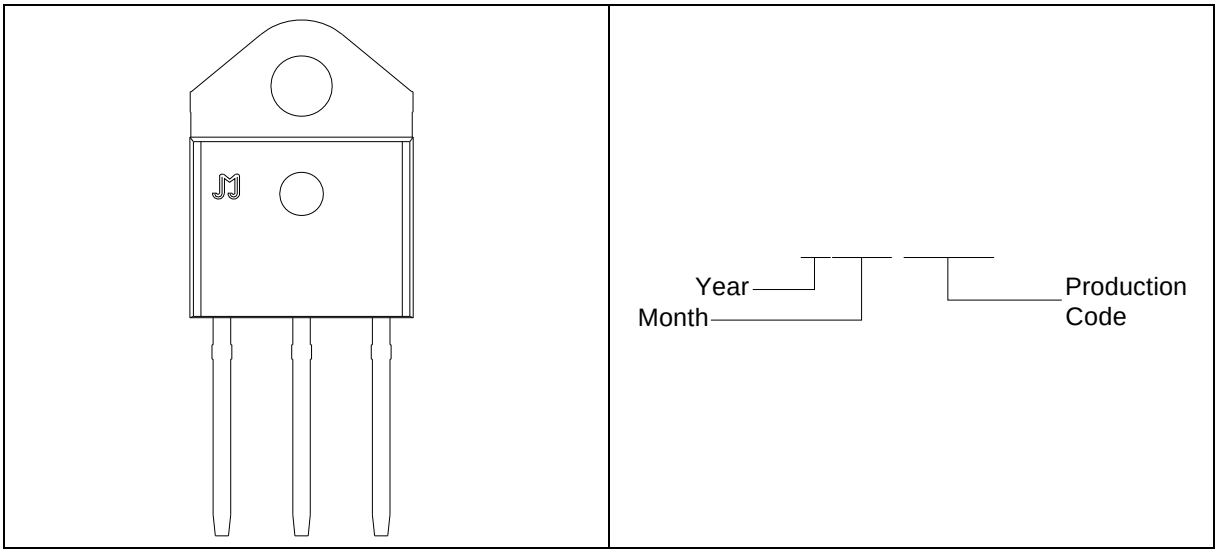
Peak gate current (t_p=20μs , T_j=125)	I_{GM}	10	A
Average gate power dissipation (T_j=125)	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	20	W
Peak pulse voltage (T_j=25 ; non-repetitive,off-state;FIG.7)	V_{pp}	0.7	kV

(T_j=25 unless otherwise specified)

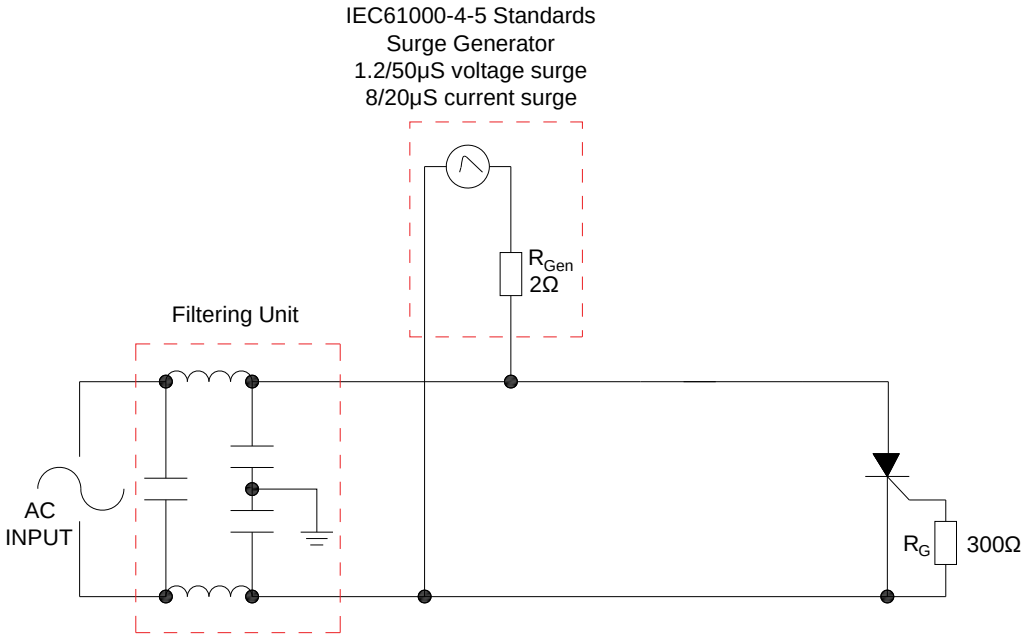
Symbol	Test Condition	Value			Unit
		MIN.	TYP.	MAX.	
I_{GT}	V_D=12V R_L=33Ω	-	-	45	mA
V_{GT}		-	-	1	V
V_{GD}	V_D=V_{DRM} T_j=125 R_L=3.3kΩ	0.2	-	-	V
I_L	I_G=1.2I_{GT}	-	-	120	mA
I_H	I_T=500mA	-	-	100	mA
dV/dt	V_D=800V Gate Open T_j=125	1500	-	-	V/μs
t_{on}	I_G=50mA I_A=500mA I_R=50mA T_j=25 G	-	5	-	μs


J
CT
12
40
Z
JieJie Microelectronics Co., Ltd.
SCRs
12:VDRM /VRRM 1200V
IT(RMS):40A
Z:TO-3P(Ins)


Year
Month
Production
Code

JCT1240Z

FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards.

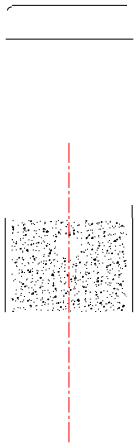


Refer to the application note “Assembly Instructions for Thyristors in Through-hole Package” released by JieJie

Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
JCT1240Z	1200	45	TO-3P(Ins)	30	Tube

Document Revision History

Date	Revision	Changes
Apr.13, 2023	A.1.0	Last update
Oct.16, 2025	A.1.1	Revise PACKAGE MECHANICAL DATA



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